

PATENTAmendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application in which added matter is underlined and deleted matter is shown using ~~striketrough~~ unless striketrough is unclear or ambiguous in which case deleted matter is shown in [square brackets]:

Listing of Claims:

1. (Original) A startup circuit for a power converter, the power converter including ~~an error amplifier that compares an output sense signal with a startup reference signal and that provides a compensation signal indicative thereof, the~~ startup circuit comprising:  
an amplifier circuit that charges the startup reference signal to a predetermined reference level based on a second reference signal in response to a start signal;  
a comparator that determines when the compensation signal reaches a predetermined ramp level and that asserts a startup complete signal indicative thereof; and  
startup logic that provides said start signal and that provides an output enable signal in response to said startup complete signal.
2. (Original) The startup circuit of claim 1, wherein said predetermined ramp level is approximately the center voltage of a sawtooth regulation waveform used for PWM modulation.
3. (Currently Amended) The startup circuit of claim 1, wherein said amplifier circuit comprises:  
an amplifier, having an input receiving said second reference signal, and an output; and  
a capacitor coupled to said output of said amplifier;  
wherein said amplifier charges said capacitor in response to said start signal to charge said startup reference signal.

PATENT

4. (Original) The startup circuit of claim 3, further comprising a first switch coupled across said capacitor, wherein said start signal opens said first switch to enable charging of said capacitor.
5. (Original) The startup circuit of claim 4, further comprising:  
a second switch coupled in a feedback path of said amplifier, and  
wherein said second switch is initially open to place said amplifier in an open loop configuration, and wherein said second switch is closed to switch said amplifier into a closed loop configuration to maintain said startup reference signal based on said second reference signal.
6. (Original) The startup circuit of claim 5, further comprising:  
said amplifier having a first input receiving said second reference signal and a second input coupled to said second switch; and  
a third switch coupled between said second input of said amplifier and ground, wherein said third switch is closed during startup operations and while said amplifier is charging said capacitor and wherein said third switch is opened when said second switch is closed.
7. (Original) The startup circuit of claim 6, wherein said startup logic comprises a digital state machine that controls said first, second and third switches to startup said power converter.
8. (Original) The startup circuit of claim 6, wherein said amplifier comprises an operational transconductance amplifier.
9. (Original) The startup circuit of claim 6, further comprising:  
a first voltage follower having an input receiving said second reference signal and an output coupled to said first input of said amplifier; and  
a second voltage follower having an input coupled to said second and third switches and an output coupled to said second input of said amplifier.
10. (Original) The startup circuit of claim 9, further comprising:  
a first resistor coupled between said output of said first voltage follower and said first input of said amplifier;  
a second resistor coupled between said output of said second voltage follower and said second input of said amplifier; and

PATENT

a margin controller coupled to adjust current through said first and second resistors.

11. (Currently Amended) A controller for a power converter, comprising:  
an error amplifier having a first input receiving an output sense signal, a second input receiving a startup reference signal and an output that provides a compensation signal;  
a comparator having inputs for comparing said compensation signal with a predetermined ramp level and an output for providing a startup complete signal;  
gate control logic that controls output switching of said power converter and that disables output switching ~~based on~~ when an output enable signal is negated and that enables output switching when said output enable signal is asserted; and  
a startup circuit, coupled to said error amplifier and providing said output enable signal, that controls initiation of said error amplifier including charging of said startup reference signal and that ~~disables output switching negates said output enable signal~~ until said compensation signal achieves an operative level startup complete signal is provided.
12. (Currently Amended) The controller of claim 11, wherein said ~~startup circuit comprises a comparator having inputs for comparing said compensation signal with a~~ predetermined ramp level is based on a PWM triangular waveform and an output for providing a wherein said startup complete signal is provided when said compensation signal achieves an operative level.
13. (Original) The controller of claim 12, wherein said predetermined ramp level is a voltage level placed at approximately the center of said triangular waveform.
14. (Currently Amended) The controller of claim 11, wherein said startup circuit comprises:  
a capacitor, coupled to said second input of said error amplifier, that develops said startup reference signal; and

PATENT

an amplifier, having an input receiving a voltage reference signal and an output coupled to said capacitor, wherein said amplifier operates in a first state to charge said capacitor and operates in a second state to regulate said startup reference signal based on said voltage reference signal.

15. (Currently Amended) The controller of claim 14, wherein said startup circuit further comprises:
  - a plurality of switches coupled to said amplifier and said capacitor; and
  - a digital state machine that controls said plurality of switches to determine operative states, including said first and second states, of said amplifier.
16. (Original) The controller of claim 15, wherein:
  - said amplifier has a first input receiving said voltage reference signal and a second input;
  - wherein said capacitor is coupled between said output of said amplifier and ground; and
  - wherein said plurality of switches comprises:
    - a first switch coupled across said capacitor;
    - a second switch coupled between said second input and said output of said amplifier; and
    - a third switch coupled between said second input of said amplifier and ground.
17. (Original) The controller of claim 16, wherein said digital state machine opens said first and second switches and closes said third switch for said first state, and wherein said digital state machine closes said second switch and opens said third switch for said second state.
18. (Currently Amended) The controller of claim 17, wherein said digital state machine closes said first and third switches and opens said second switch for a third reset state.
19. (Original) The controller of claim 14, wherein said amplifier comprises an operational transconductance amplifier.
20. (Currently Amended) A method of startup protection for a DC-DC converter, comprising:

PATENT

disabling output switching of the DC-DC converter;  
ramping up voltage of a reference input of an error amplifier based on a reference signal;  
providing, by the error amplifier, a compensation signal based on the reference input and a feedback portion of an output of the DC-DC converter;  
comparing the compensation signal with a predetermined ramp level and  
providing a startup complete signal indicative thereof; and  
enabling the output switching of the DC-DC converter when the ~~compensation~~ signal reaches a predetermined regulation level startup complete signal is  
provided.

21. (Currently Amended) The method of claim 20, wherein said ramping up voltage of ~~a~~ the reference input of the error amplifier comprises charging a capacitor by an operational transconductance amplifier (OTA).
22. (Currently Amended) The method of claim 210, further comprising:  
providing the reference signal to an input of the OTA;  
operating the OTA in an open loop state to charge the capacitor; and  
operating the OTA in a closed loop state when regulation is achieved to maintain voltage of the capacitor based on the reference signal.